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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/830,376	04/25/2001	Yoshikazu Satoh	PHJ 99,016	7757

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EXAMINER	
CHERY, MARDOCHEE	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 02/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/830,376	YOSHIKAZU SATOH	
	Examiner	Art Unit	
	Mardochee Chery	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/25/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to Application No. 09/830,376 filed on April 25, 2001.

Information Disclosure Statement

2. The information disclosure statement filed 04/25/01 fails to comply with 37 CFR 1.98(a)(1), which requires a list of all patents, publications, or other information submitted for consideration by the Office. The following documents: EP 0963073 A1 and 0186139 A2 have been placed in the application file, but the information referred to therein has not been considered.

Oath/Declaration

3. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:

a. It does not identify the foreign application for patent or inventor's certificate on which priority is claimed pursuant to 37 CFR 1.55, and any foreign application having a filing date before that of the application on which priority is claimed, by specifying the application number, country, day, month and year of its filing.

b. It was not executed in accordance with either 37 CFR 1.66 or 1.68.

c. The full name of each inventor (family name and at least one given name together with any initial) has not been set forth.

d. It does not state that the person making the oath or declaration believes the named inventor or inventors to be the original and first inventor or inventors of the subject matter which is claimed and for which a patent is sought.

e. It does not identify the foreign application for patent or inventor's certificate on which priority is claimed pursuant to 37 CFR 1.55, and any foreign application having a filing date before that of the application on which priority is claimed, by specifying the application number, country, day, month and year of its filing.

f. It does not identify the citizenship of each inventor.

g. It does not identify the city and either state or foreign country of residence of each inventor. The residence information may be provided on either on an application data sheet or supplemental oath or declaration.

h. Receipt is acknowledged of papers filed under 35 U.S.C. 119 (a)-(d) based on an application filed in Japan on 8/26/99. Applicant has not complied with the requirements of 37 CFR 1.63(c), since the oath, declaration or application data sheet does not acknowledge the filing of any foreign application.

Abstract

4. The abstract of the disclosure is objected to because:

the abstract does not comply with the proper content, format, and language outlined in MPEP §.608.01(b). Applicant is reminded of the proper content of an abstract of the disclosure. The following guidelines illustrate the preferred layout for the abstract of a utility application. These guidelines are suggested for the applicant's use.

a. A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If

the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

b. The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:

(1) if a machine or apparatus, its organization and operation;

(2) if an article, its method of making;

(3) if a chemical compound, its identity and use;

(4) if a mixture, its ingredients;

(5) if a process, the steps.

c. The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space

provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

d. The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Correction is required. See MPEP § 608.01(b).

Specification

4. The disclosure is objected to because of the following informalities:

a) On page 2, line 13, it appears that "the read of data" should be changed to –the reading of data--.

b) On page 5, line 21, it appears that "An de-interleaving method" should be changed to –A de-interleaving method--.

I. Arrangement of the Specification

The arrangement of the disclosure does not contain the different sections as outlined in rule 37 CFR 1.154. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.

(b) CROSS-REFERENCE TO RELATED APPLICATIONS.

(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.

(d) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or

REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)

(e) BACKGROUND OF THE INVENTION.

(1) Field of the Invention.

(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.

(f) BRIEF SUMMARY OF THE INVENTION.

(g) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).

(h) DETAILED DESCRIPTION OF THE INVENTION.

(i) CLAIM OR CLAIMS (commencing on a separate sheet).

(j) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).

(k) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

II. Content of Specification

(a) Title of the Invention: See 37 CFR 1.72(a) and MPEP § 606. The title of the invention should be placed at the top of the first page of the specification unless the title is provided in an application data sheet. The title of the invention should be brief but technically accurate and

descriptive, preferably from two to seven words may not contain more than 500 characters.

(b) Cross-References to Related Applications: See 37 CFR 1.78 and MPEP § 201.11.

(c) Statement Regarding Federally Sponsored Research and Development: See MPEP § 310.

(d) Incorporation-By-Reference Of Material Submitted On a Compact Disc: The specification is required to include an incorporation-by-reference of electronic documents that are to become part of the permanent United States Patent and Trademark Office records in the file of a patent application. See 37 CFR 1.52(e) and MPEP § 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text were permitted as electronic documents on compact discs beginning on September 8, 2000.

Or alternatively, Reference to a "Microfiche Appendix": See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.

(e) Background of the Invention: See MPEP § 608.01(c). The specification should set forth the Background of the Invention in two parts:

(1) Field of the Invention: A statement of the field of art to which the invention pertains. This statement may include a paraphrasing of the applicable U.S. patent classification definitions of the subject matter of the claimed invention. This item may also be titled "Technical Field."

(2) Description of the Related Art including information disclosed under 37 CFR 1.97 and 37 CFR 1.98: A description of the related art known to the applicant and including, if applicable, references to specific related art and problems involved in the prior art which are solved by the applicant's invention. This item may also be titled "Background Art."

(f) Brief Summary of the Invention: See MPEP § 608.01(d). A brief summary or general statement of the invention as set forth in 37 CFR 1.73. The summary is separate and distinct from the abstract and is directed toward the invention rather than the disclosure as a whole. The summary may point out the advantages of the invention or how it solves problems previously existent in the prior art (and preferably indicated in the

Background of the Invention). In chemical cases it should point out in general terms the utility of the invention. If possible, the nature and gist of the invention or the inventive concept should be set forth. Objects of the invention should be treated briefly and only to the extent that they contribute to an understanding of the invention.

(g) Brief Description of the Several Views of the Drawing(s): See MPEP § 608.01(f). A reference to and brief description of the drawing(s) as set forth in 37 CFR 1.74.

(h) Detailed Description of the Invention: See MPEP § 608.01(g). A description of the preferred embodiment(s) of the invention as required in 37 CFR 1.71. The description should be as short and specific as is necessary to describe the invention adequately and accurately. Where elements or groups of elements, compounds, and processes, which are conventional and generally widely known in the field of the invention described and their exact nature or type is not necessary for an understanding and use of the invention by a person skilled in the art, they should not be described in detail. However, where particularly complicated subject matter is involved or where the elements, compounds, or processes may not be commonly or widely known in the field, the specification should refer to another patent or readily available publication which adequately describes the subject matter.

(i) Claim or Claims: See 37 CFR 1.75 and MPEP § 608.01(m). The claim or claims must commence on separate sheet or electronic page (37 CFR 1.52(b)(3)). Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation. There may be plural indentations to further segregate subcombinations or related steps. See 37 CFR 1.75 and MPEP § 608.01(i)-(p).

(j) Abstract of the Disclosure: See MPEP § 608.01(f). A brief narrative of the disclosure as a whole in a single paragraph of 150 words or less commencing on a separate sheet following the claims. In an international application which has entered the national stage (37 CFR 1.491(b)), the applicant need not submit an abstract commencing on a separate sheet if an abstract was published with the international application under PCT Article 21. The abstract that appears on the cover page of the pamphlet published by the International Bureau (IB) of the World Intellectual Property Organization (WIPO) is the abstract that will be used by the USPTO. See MPEP § 1893.03(e).

(k) Sequence Listing, See 37 CFR 1.821-1.825 and MPEP §§ 2421-2431. The requirement for a sequence listing applies to all sequences disclosed

in a given application, whether the sequences are claimed or not. See MPEP § 2421.02.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 1-3, and 15-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Higashida et al. (6,826,181).

As per claim 1, Higashida et al. discloses a data writing/reading method of sequentially writing a plurality of data into a memory in a write direction [*the generating*

means executes the interleave process by writing the data; col.3, lines 34-35; *buffer memory 3000 in a first direction (write direction of Fig.21 (C)*; col.24, lines 50-51; *data into a plurality of blocks (plurality of data)*; col.2, lines 46-47]; and sequentially reading the plurality of data written into the memory in a read direction [*for the reading, the interleave control circuit 1003 generates an address and sequentially reads the data*; col.21, lines 65-67; *memory 3000 in a second direction (read direction of Fig. 21(C))*; col.24, lines 53-55; *data into a plurality of blocks*; col.2, lines 46-47]; characterized in that a first plurality of data is written into the memory in a first write direction [*writing the data into the storage apparatus having a matrix form in a first direction*; col.3, lines 35-37]; the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction [*packet transmission (plurality of data)*; col.3, lines 27-28; *writing the data into a storage apparatus having a matrix form in a first direction, reading from the storage apparatus the data in a second direction perpendicular to the first direction of the matrix*; col.3, lines 35-39].

As per claim 2, Higashida et al. discloses when plural data having written into the memory at present are read in a row direction, plural data which is the next to be written are sequentially written in the row direction [*packet transmission (plurality of data)*; col.3, lines 27-28; *128-bytes data is written into memory 1002 in the row direction 9001 of Fig.17 and executes the writing of data*; col.21, lines 57-60], on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction [*data are sequentially written in the row direction, and when the writing of data into each row is completed, writing of data in the row direction of*

the next column is executed; reading is executed in a unit in the column direction; Fig.20, col.23, lines 38-46].

As per claim 3, Higashida et al. discloses plural data are arranged into the memory in matrix structures having n by n blocks [*a storage apparatus having a matrix form*; col.3, lines 36-37]; each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks [*when the writing of data into each column is completed, the writing is advanced in the column direction of the data in a direction in which the row address increases*; col.38, lines 6-9].

As per claim 15, Higashida et al. discloses a memory for sequentially writing a plurality of data into a memory in a write direction [*the generating means executes the interleave process by writing the data*; col.3, lines 34-35; *buffer memory 3000 in a first direction (write direction of Fig.21 (C)*; col.24, lines 50-51; *data into a plurality of blocks (plurality of data)*; col.2, lines 46-47]; and sequentially reading the plurality of data written into the memory in a read direction [*for the reading, the interleave control circuit 1003 generates an address and sequentially reads the data*; col.21, lines 65-67; *memory 3000 in a second direction (read direction of Fig: 21(C))*; col.24, lines 53-55; *data into a plurality of blocks*; col.2, lines 46-47]; characterized in that a first plurality of data is written into the memory in a first write direction [*writing the data into the storage apparatus having a matrix form in a first direction*; col.3, lines 35-37]; the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data

in a second write direction which is equal to or is opposite to the first read direction [*packet transmission (plurality of data)*; col.3, lines 27-28; *writing the data into a storage apparatus having a matrix form in a first direction, reading from the storage apparatus the data in a second direction perpendicular to the first direction of the matrix*; col.3, lines 35-39].

As per claim 16, Higashida et al. discloses a memory drive apparatus [*transmission and storage apparatus*; col.3, lines 45-48]; sequentially writing a plurality of data into a memory in a write direction [*the generating means executes the interleave process by writing the data*; col.3, lines 34-35; *buffer memory 3000 in a first direction (write direction of Fig.21 (C)*; col.24, lines 50-51; *data into a plurality of blocks (plurality of data)*; col.2, lines 46-47]; and sequentially reading the plurality of data written into the memory in a read direction [*for the reading, the interleave control circuit 1003 generates an address and sequentially reads the data*; col.21, lines 65-67; *memory 3000 in a second direction (read direction of Fig. 21(C))*; col.24, lines 53-55; *data into a plurality of blocks*; col.2, lines 46-47]; characterized in that a first plurality of data is written into the memory in a first write direction [*writing the data into the storage apparatus having a matrix form in a first direction*; col.3, lines 35-37]; the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction [*packet transmission (plurality of data)*; col.3, lines 27-28; *writing the data into a storage apparatus having a matrix form in a first direction, reading from the storage apparatus the data in a second direction perpendicular to the first direction of the matrix*; col.3, lines 35-39].

As per claim 17, Higashida et al. discloses when plural data having written into the memory at present are read in a row direction, plural data which is the next to be written are sequentially written in the row direction [*packet transmission (plurality of data)*; col.3, lines 27-28; *128-bytes data is written into memory 1002 in the row direction 9001 of Fig.17 and executes the writing of data*; col.21, lines 57-60], on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction [*data are sequentially written in the row direction, and when the writing of data into each row is completed, writing of data in the row direction of the next column is executed; reading is executed in a unit in the column direction*; Fig.20, col.23, lines 38-46].

As per claim 18, Higashida et al. discloses the apparatus provides with addressing means for addressing the memory [*the interleave control circuit 1003 generates an address and sequentially reads the data*; col.21, lines 65-67]; plural data are arranged into the memory in matrix structures having n by n blocks [*a storage apparatus having a matrix form*; col.3, lines 36-37]; each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks [*when the writing of data into each column is completed, the writing is advanced in the column direction of the data in a direction in which the row address increases*; col.38, lines 6-9].

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higashida et al. (6,826,181) in view of Biro et al. (5,995,080).

As per claim 4, Higashida et al. discloses a data writing/reading method of sequentially writing a plurality of data into a memory in a write direction [*the generating means executes the interleave process by writing the data*; col.3, lines 34-35; *buffer memory 3000 in a first direction (write direction of Fig.21 (C)*; col.24, lines 50-51; *data into a plurality of blocks (plurality of data)*; col.2, lines 46-47]; and sequentially reading the plurality of data written into the memory in a read direction [*for the reading, the interleave control circuit 1003 generates an address and sequentially reads the data*; col.21, lines 65-67; *memory 3000 in a second direction (read direction of Fig. 21(C))*; col.24, lines 53-55; *data into a plurality of blocks*; col.2, lines 46-47]; characterized in that a first plurality of data is written into the memory in a first write direction [*writing the data into the storage apparatus having a matrix form in a first direction*; col.3, lines 35-37]; the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite

to the first read direction [*packet transmission (plurality of data)*; col.3, lines 27-28; *writing the data into a storage apparatus having a matrix form in a first direction, reading from the storage apparatus the data in a second direction perpendicular to the first direction of the matrix*; col.3, lines 35-39].

However Higashida et al. does not specifically teach a method of de-interleaving. Biro et al. discloses a method of de-interleaving [*a method for providing de-interleaving of data using a storage device*; col.2, lines 63-65] to provide output data that is stored in an interleaved format to other logic in a block format while using a minimal amount of additional hardware (col.3, lines 8-12).

Since the technology for implementing a storage system with a method of de-interleaving was well known as evidenced by Biro et al., and since a method of de-interleaving in a storage system provides output data that is stored in an interleaved format to other logic in a block format while using a minimal amount of additional hardware, an artisan would have been motivated to implement this feature in the system of Higashida et al.. Thus, it would have been obvious to one of ordinary skill in the art at the time invention was made by applicant, to modify the system of Higashida et al. to include a method of de-interleaving because it was well known to provide output data that is stored in an interleaved format to other logic in a block format while using a minimal amount of additional hardware (col.3, lines 8-12) as taught by Biro et al..

As per claim 5, Higashida et al. discloses when plural data having written into the memory at present are read in a row direction, plural data which is the next to be written are sequentially written in the row direction [*packet transmission (plurality of data)*; col.3, lines 27-28; *128-bytes data is written into memory 1002 in the row direction 9001 of Fig.17 and executes the writing of data*; col.21, lines 57-60], on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction [*data are sequentially written in the row direction, and when the writing of data into each row is completed, writing of data in the row direction of the next column is executed; reading is executed in a unit in the column direction*; Fig.20, col.23, lines 38-46].

As per claim 6, Higashida et al. discloses plural data are arranged into the memory in matrix structures having n by n blocks [*a storage apparatus having a matrix form*; col.3, lines 36-37]; each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks [*when the writing of data into each column is completed, the writing is advanced in the column direction of the data in a direction in which the row address increases*; col.38, lines 6-9].

As per claim 7, Higashida et al. discloses a data processing method (Fig.4, *data processing circuit 104*; col.6, lines 42-43; *the transmission can be achieved by executing the process twice;* col.22, lines 33-34]; a first step of interleaving a plurality of data [*data into a plurality of blocks; a first processing means for executing a first interleave process*; col.3, lines 43-47];

sequentially writing a plurality of data into a memory in a write direction [*the generating means executes the interleave process by writing the data*; col.3, lines 34-35; *buffer memory 3000 in a first direction (write direction of Fig.21 (C)*; col.24, lines 50-51; *data into a plurality of blocks (plurality of data)*; col.2, lines 46-47]; and sequentially reading the plurality of data written into the memory in a read direction [*for the reading, the interleave control circuit 1003 generates an address and sequentially reads the data*; col.21, lines 65-67; *memory 3000 in a second direction (read direction of Fig. 21(C))*; col.24, lines 53-55; *data into a plurality of blocks*; col.2, lines 46-47]; characterized in that a first plurality of data is written into the memory in a first write direction [*writing the data into the storage apparatus having a matrix form in a first direction*; col.3, lines 35-37]; the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction [*packet transmission (plurality of data)*; col.3, lines 27-28; *writing the data into a storage apparatus having a matrix form in a first direction, reading from the storage apparatus the data in a second direction perpendicular to the first direction of the matrix*; col.3, lines 35-39].

However, Higashida et al. does not specifically teach a second step of de-interleaving. Biro et al. discloses a second step of de-interleaving [to *provide de-interleaving, the first order of bytes includes a plurality of interleaved bytes of different types of data, and the second output order of bytes comprises a plurality of bytes of the same type of data;* col.3, lines 1-4] to provide output data that is stored in an interleaved format to other logic in a block format while using a minimal amount of additional hardware (col.3, lines 8-12).

Since the technology for implementing a storage system with a second step of de-interleaving was well known as evidenced by Biro et al., and since a second step of de-interleaving in a storage system provides output data that is stored in an interleaved format to other logic in a block format while using a minimal amount of additional hardware, an artisan would have been motivated to implement this feature in the system of Higashida et al.. Thus, it would have been obvious to one of ordinary skill in the art at the time invention was made by applicant, to modify the system of Higashida et al. to include a second step of de-interleaving because it was well known to provide output data that is stored in an interleaved format to other logic in a block format while using a minimal amount of additional hardware (col.3, lines 8-12) as taught by Biro et al..

As per claim 8, Higashida et al. discloses when plural data having written into the memory at present are read in a row direction, plural data which is the next to be written are sequentially written in the row direction [*packet transmission (plurality of data)*; col.3, lines 27-28; *128-bytes data is written into memory 1002 in the row direction 9001 of Fig.17 and executes the writing of data*; col.21, lines 57-60], on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction [*data are sequentially written in the row direction, and when the writing of data into each row is completed, writing of data in the row direction of the next column is executed; reading is executed in a unit in the column direction*; Fig.20, col.23, lines 38-46].

As per claim 9, Higashida discloses the first step contains configuring a super frame having plural frames, each of the frames formed by arranging plural data in matrix form, and contains interleaving the plural data configuring the super frame [*execute the interleave process by writing data into a storage having a matrix form*; col.3, lines 34-37; *a first interleave processing means for executing a first interleave process by writing data into a first storage having a first matrix form; second interleave processing means for executing a second interleave process by writing data into a second storage having a second matrix form; each storage (frame) stores matrix/matrices which store(s) plural data*; col3, lines 46-61].

As per claim 10, Higashida et al. discloses plural data are arranged into the memory in matrix structures having n by n blocks [*a storage apparatus having a matrix form*; col.3, lines 36-37]; each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks [*when the writing of data into each column is completed, the writing is advanced in the column direction of the data in a direction in which the row address increases*; col.38, lines 6-9].

As per claim 11, Higashida et al. discloses when plural data having written into the memory at present are read in a row direction, plural data which is the next to be written are sequentially written in the row direction [*packet transmission (plurality of data)*; col.3, lines 27-28; *128-bytes data is written into memory 1002 in the row direction 9001 of Fig.17 and executes the writing of data*; col.21, lines 57-60], on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction [*data are sequentially*

written in the row direction, and when the writing of data into each row is completed, writing of data in the row direction of the next column is executed; reading is executed in a unit in the column direction;

Fig.20, col.23, lines 38-46].

Regarding claim 11, although Higashida et al. and Biro et al. do not specifically teach each of the frames formed by arranging (203x48) data in matrix form, and interleaving (203x48x8) data, such limitations are merely a matter of design choice and would have been obvious in the system of Higashida et al.. Higashida et al. teaches a two-dimensional matrix, and the frames become the multiple of 48 bytes to execute the interleave process and express data write and read control. The limitations in claim 11 do not define a patentably distinct invention over that in Higashida et al. since both the invention as a whole and Higashida et al. are directed to configuring and interleaving the super frame. The size of the data in the matrix is inconsequential for the invention as a whole and presents no new or unexpected results, as long as the data is in matrix form. Therefore, to have each of the frames formed by arranging (203x48) data in matrix form, and interleaving (203x48x8) data would have been a matter of obvious design choice to one of ordinary skill in the art.

As per claims 12-14, the rationale in the rejection of claim 10 is herein incorporated.

Regarding claims 12-14, although Higashida et al. and Biro et al. do not specifically teach a super frame having eight frames, each of the frames formed by arranging (203x48) data in matrix form, interleaving (203x48x8) data, and each block having 4 or 26 addresses, such limitations are merely a matter of design choice and would have been obvious in the system of Higashida et al.. Higashida et al. teaches a two-dimensional matrix, and the frames become the multiple of 48 bytes, to execute the interleave process and express data write and read control, and control circuit 1003 generates an address to sequentially read the data in the row direction of the matrix. The limitations in claims 12-14 do not define a patentably distinct invention over that in Higashida et al. since both the invention as a whole and Higashida et al. are directed to configuring, interleaving the super frame, and sequentially reading the data. The size of the data in the matrix is inconsequential for the invention as a whole and presents no new or unexpected results, as long as the data is in matrix form. Therefore, to have each of the frames formed by arranging (203x48) data in matrix form, and interleaving (203x48x8) data would have been a matter of obvious design choice to one of ordinary skill in the art.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Higashida et al.	6,826,181
Biro et al.	5,995,080
Norbert et al.	3,271,749

10. When responding to the office action, Applicant is advised to clearly point out the patentable novelty that he or she thinks the claims present in view of the state of the art disclosed by references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c).

11. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee Chery whose telephone number is (571)272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Manonama Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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